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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,555	01/11/2002	Thomas Michael Anderson	CE04890N	9501

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MOTOROLA, INC.
LAW DEPARTMENT
1303 E. ALGONQUIN ROAD
SCHAUMBURG, IL 60196

EXAMINER	
WASEL, MOHAMED A	
ART UNIT	**PAPER NUMBER**
2154	

DATE MAILED: 03/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,555	ANDERSON ET AL.	
	Examiner	Art Unit	
	Mohamed Wasel	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *18-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/25/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to Election/ Restriction Requirement filed on November 14, 2005.

Claims 1-27 are pending.

Claims 18-27 have been withdrawn.

Applicant elects to prosecute, without traverse, Claims 1-17.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Dea et al, (Dea) U.S. Patent No. 5,742,833.

1. As per claim 1, Dea teaches a method of communicating over a controller area network (CAN) bus, comprising:

a) routing registration information from a plurality of processor-enabled peripheral devices to a controlling software component (***col. 3 lines 20-24, col.7 lines 35-52***);

b) routing a periodic heartbeat message from the controlling software component to the plurality of processor-enabled peripheral devices to enable each of the plurality of processor-enabled peripheral devices to maintain its registered status (***col. 7 lines 35-52***); and

c) if necessary, routing messages from the controlling software component to one or more of the plurality of processor-enabled peripheral devices on a discrete basis over the CAN bus to control the one or more of the plurality of processor-enabled peripheral devices (***col. 3 lines 20-24, col. 6 lines 7-28***).

2. As per claim 2, Dea teaches the method further comprising causing the controlling software component to consecutively receive frames of a multi-frame message transmitted from one of the plurality of processor-enabled peripheral devices (***col. 7 lines 36-53***).

3. As per claim 3, Dea teaches the method wherein the routing of messages from the controlling software component to one or more of the plurality of processor-enabled peripheral devices on a discrete basis to control the one or more of the plurality of processor-enabled peripheral devices comprises routing messages each having a like header to the one or more of the plurality of processor-enabled peripheral devices on a discrete basis to control the one or more of the plurality of processor-enabled peripheral devices (***col. 7 lines 36-53, col. 9 lines 19-48***).

4. As per claim 4, Dea teaches the method wherein the routing of messages each having a like header to one or more of the plurality of processor-enabled peripheral devices on a discrete basis to control the one or more of the plurality of processor-enabled peripheral devices comprises routing messages each having a common header component and a CAN header component to the one or more of the plurality of processor-enabled peripheral devices on a

discrete basis to control the one or more of the plurality of processor-enabled peripheral devices (***col. 7 lines 36-53, col. 9 lines 19-48***).

5. As per claim 5, Dea teaches the method wherein the routing of messages each having a common header component and a CAN header component to the one or more of the plurality of processor-enabled peripheral devices on a discrete basis to control the one or more of the plurality of processor-enabled peripheral devices further comprises routing messages each having a common header component and a CAN header component without specific knowledge by the controlling software component of the CAN header component (***col. 7 lines 36-53, col. 9 lines 19-48***).

6. As per claim 6, Dea teaches a method of communicating over a controller area network (CAN) bus, comprising:

a) routing a registration message from a processor-enabled peripheral device to a controlling software component (***col. 3 lines 20-24, col.7 lines 35-52***);

b) at the processor-enabled peripheral device, periodically receiving a heartbeat message from the controlling software component subsequent to the routing of a registration message from a processor-enabled peripheral device to a controlling software component (***col. 7 lines 35-52***); and

c) receiving at the processor-enabled peripheral device discrete control messages that are transmitted from the controlling software component (***col. 3 lines 20-24, col. 6 lines 7-28***).

7. As per claim 7, Dea teaches the method wherein the receiving at the processor-enabled peripheral device discrete control messages that are transmitted from the controlling software component comprises filtering the transmitted control messages at the processor-enabled peripheral device to enable only the discrete control messages intended specifically for the processor-enabled peripheral device to reach the processor-enabled peripheral device (***col. 7 lines 36-53, col. 9 lines 19-48, col. 10 lines 1-11***).

8. As per claim 8, Dea teaches the method wherein the filtering of the transmitted control messages at the processor-enabled peripheral device to enable only the discrete control messages intended specifically for the processor-enabled peripheral device to reach the processor-enabled peripheral device comprises filtering the transmitted control messages at the processor-enabled peripheral device via a hardware filter to determine whether the transmitted control messages are for a certain type of processor-controlled peripheral device, and filtering the transmitted control messages at the processor-enabled peripheral device via a software filter to determine processor-controlled peripheral device numbers from respective message CAN headers (***col. 3 lines 34-38, col. 10 lines 1-11***).

9. As per claim 9, Dea teaches the method further comprising receiving at the processor-enabled peripheral device all message frames following the processor-enabled peripheral device type and number information subsequent to the filtering of processor-enabled peripheral device type and number information from the discrete control messages intended specifically for the processor-enabled peripheral device (***col. 9 lines 6-18***).

10. As per claim 10, Dea teaches the method wherein the filtering the transmitted control messages at the processor-enabled peripheral device to enable only the discrete control messages intended specifically for the processor-enabled peripheral device to reach the processor-enabled peripheral device is invisible with respect to the controlling software component (***col. 9 lines 49-64***).

11. As per claim 11, Dea teaches the method further comprising, at the processor-enabled peripheral device, consecutively receiving frames of a multi-frame discrete control message (***col. 7 lines 36-53, col. 9 lines 19-48, col. 9 lines 6-18***).

12. As per claim 12, Dea teaches a controller area network (CAN) bus for enabling a controlling software component to communicate discretely with each of a plurality of processor-enabled peripheral devices irrespective of whether the processor-enabled peripheral devices are like devices (***col. 5 lines 1-16***), comprising:

a) a processor for routing control messages between the controlling software component and the plurality of processor-enabled peripheral devices (***col. 6 lines 7-28***);

b) a plurality of bus lines for connecting the processor to the controlling software component and the plurality of processor-enabled peripheral devices (***col. 6 lines 7-28***); and

c) the processor for enabling the control messages to be discretely transmitted from the controlling software component to one or more of the plurality of processor-enabled peripheral devices (***col. 4 line 61 to col. 5 line 16***).

13. As per claim 13, Dea teaches the CAN bus wherein the processor is programmed with a software switch for enabling the controlling software component to consecutively receive frames of a multi-frame message transmitted from one of the plurality of processor-enabled peripheral devices (***col. 7 lines 36-53, col. 9 lines 6-18***).

14. As per claim 14, Dea teaches the CAN bus wherein the processor is programmed for enabling transmission of multi-frame CAN bus messages (***col. 9 lines 6-18***).

15. As per claim 15, Dea teaches the CAN bus wherein the processor is further for generating a CAN header component for each of the control messages transmitted from the controlling software component to enable the control messages to be discretely transmitted from the controlling software component to one or more of the plurality of processor-enabled peripheral devices (***col. 2 line 66 to col. 3 line 10, col. 7 lines 36-53, col. 9 lines 19-48***).

16. As per claim 16, Dea teaches the CAN bus wherein the processor is further for causing frames of a multi-frame message transmitted to one of the plurality of processor-enabled peripheral devices from the controlling software component to be consecutively received at the one of the plurality of processor-enabled peripheral devices (***col. 7 lines 36-53, col. 7 lines 36-53, col. 9 lines 19-48***).

17. As per claim 17, Dea teaches the CAN bus wherein the processor and the plurality of bus lines are implemented on a controlling board of a wireless base station (***col. 6 lines 2-15***).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Please refer to form PTO-892 (*Notice of Reference Cited*) for a list of relevant prior art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohamed Wasel whose telephone number is (571) 272-2669. The examiner can normally be reached on Mon-Fri (8:00 am - 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MW
February 17, 2006

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100